CLAIMS

WHAT IS CLAIMED:

1. A built-in self-test controller, comprising a logic built-in self-test domain capable of performing a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test.

2. The built-in self-test controller of claim 1, wherein the logic built-in self-test domain comprises:

a logic built-in self-test state machine; and

a pattern generator capable of generating a scan pattern for use in a state of the logic built-in self-test state machine.

3. The built-in self-test controller of claim 2, wherein the logic built-in self-test state machine further comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and

a done state entered into from the step state when the content of the pattern generator equals the predetermined vector count.

4. The built-in self-test controller of claim 2, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

5. The built-in self-test controller of claim 2, wherein the logic built-in self-test signature includes at least one of:

a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test run.

6. The built-in self-test controller of claim 1, further comprising a memory built-in self-test domain.

7. A built-in self-test controller, comprising a logic built-in self-test domain including means for performing a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test.

8. The built-in self-test controller of claim 7, wherein the means for performing the logic built-in self-test comprises:

a logic built-in self-test state machine; and

a pattern generator capable of generating a scan pattern for use in a state of the logic built-in self-test state machine.

9. The built-in self-test controller of claim 7, further comprising a memory built-in self-test domain.

10. An integrated circuit device, comprising:

a plurality of memory components;

a logic core;

a testing interface; and

a built-in self-test controller controlled through the testing interface, comprising a logic built-in self-test domain capable of performing a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test.

11. The integrated circuit device of claim 10, wherein the logic built-in self-test domain comprises:

a logic built-in self-test state machine; and

a pattern generator capable of generating a scan pattern for use in a state of the logic built-in self-test state machine.

12. The integrated circuit device of claim 11, wherein the logic built-in self-test state machine further comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and

a done state entered into from the step state when the content of the pattern generator equals the predetermined vector count.

13. The integrated circuit device of claim 11, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

14. The integrated circuit device of claim 11, wherein the logic built-in self-test signature includes at least one of:

a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test run.

15. The integrated circuit device of claim 10, wherein the built-in self-test controller further comprises a memory built-in self-test domain.

16. The integrated circuit device of claim 10, wherein testing interface comprises a Joint Test Action Group tap controller.

17. An integrated circuit device, comprising:

a plurality of memory components;

a logic core;

a testing interface; and

means for performing a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test.

18. The integrated circuit device of claim 17, wherein the performing means comprises: